Computer Organization And Design 5th Edition Solution Pdfl

Registration No:														
Total Number of Pages: 02 B.Tech													B.Tech	
PET5J 002 5 th Semester Regular Examination 2017-18														
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	Α	nswer Question No	.1 an	d 2					orv	and a	anv f	our t	from th	e rest.
		The figu												
								_						
Q1	500		ng questions: multiple type or dash fill up type									(2 x 10)		
	a)	The load instruction is mostly used to designate a transfer from memory to a processor register known as										a		
		A. Accumulator	know	n as			D	Inc	toreti	on D	wicto	ul .		
		C. Program counter					В.	Mo	man	on Ke	egiste ess R	r onict		
	b)	Memory unit access		v co	ntent	is ca		Me		auult	:33 N	cylott	-1	
	-/	A. Read only men		,			B	F	roara	mma	ble M	lemo	rv	
		C. Virtual Memory					D	. /	ssoc	iative	Men	nory		
	c)	An n-bit microproce	essor	has		Al.								
		 n-bit program c 	ounte	r			В.				regis			
		C. n-bit ALU					D.	n-t	it ins	truction	on reg	gister		
	d)	The BSA instruction A. Branch and sto	ı is		Jahar		В.	D					addre:	
		C. Branch and shi					D.						mulator	
	e)	In signed-magnitude	e bina	arv d	livisio	on. if	the d	ivide	nd is	(111	0012	and o	livisor	is
	-,	(10011)2 then the re							/	/	,-			
		A. (00100)2		-	1		E		1010	10)2				
		C. (11001)2).	(0110	00)2				
	f)	Von Neumann archi	itectu	re is										
		A. SISD							SIME					
	~1	C. MIMD In a memory-mappe	4 1/0	cuci	hom :	which			MISC		II not	ho #	oro?	
	9)	A. LDA	u i/O	Sys	tem,	WIIICI			IN	iy wi	II HOU	De u	iele:	
		C. ADD							OUT					
	h)	The time interval be A. Word-time	twee	n ad	jacen	t bits				a .	ir	1		
		A. Word-time	U	. u	T	\cup T	В.	Bit	-time	9.	ΥT	L		
		 C. Turn around tin 	ne						lice t					
	i)	A Stack-organised (uses	inst		n of		-:				
		 A. Indirect address C. Zero addressin 					B. D.			ddres	sıng ssina			
	i)			. c. n	ultin	lior r								
	11	The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be												
		A. (812)10							(-12)					
		C. (12)10					L).	(-812)10				
02		Answer the following questions: Short answer type												(2 x 10)
-		What is SRAM and DRAM?												,
	 b) List out the types in displacement addressing. 													
	c) Write the basic performance equation?													
d) What is meant by hardwired control? e) What is TLB?														
f) What is delayed branching? g) What are the problems faced in instruction pipeline?														
	h)	Give comparison bet							I/O m	арре	d I/O			

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